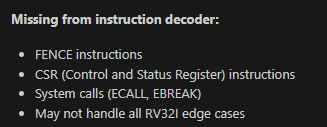
Design Weakness:

1 -Using different edges of the clock at different modules. (Is it really weakness?)

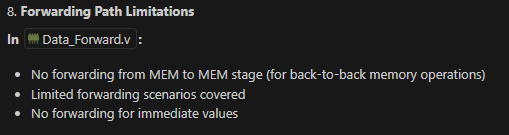
2- Memory interface problems.

3- Branch predictor is always predict branch is taken.

4-   


5- Flush signal is used as reset but using gate for reset is not reliable.

6- Limited forwarding



7- Zero Register Implementation

x0 must be always 0!!